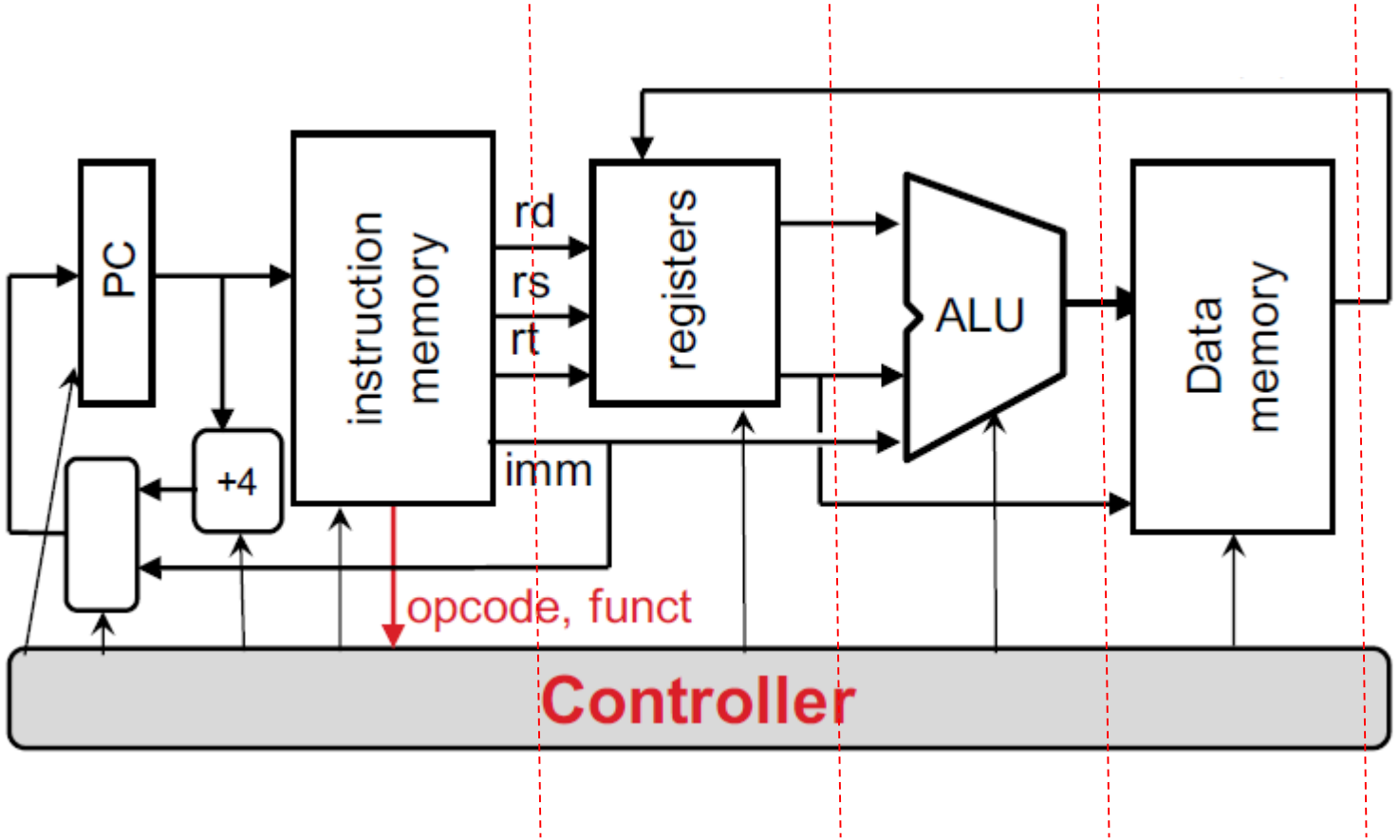
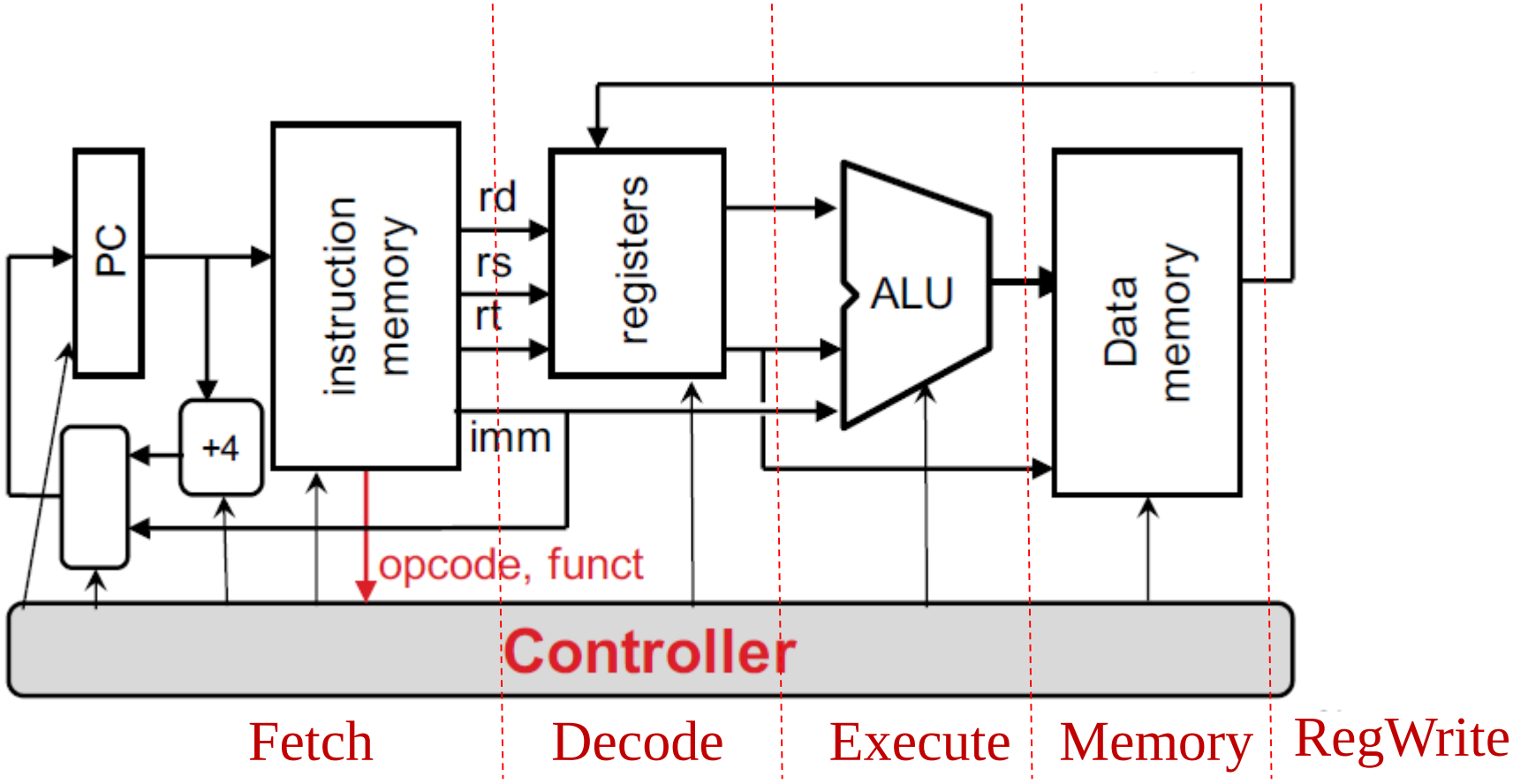
Datapath and TIPs for Processor Design

Recall five stages on datapath

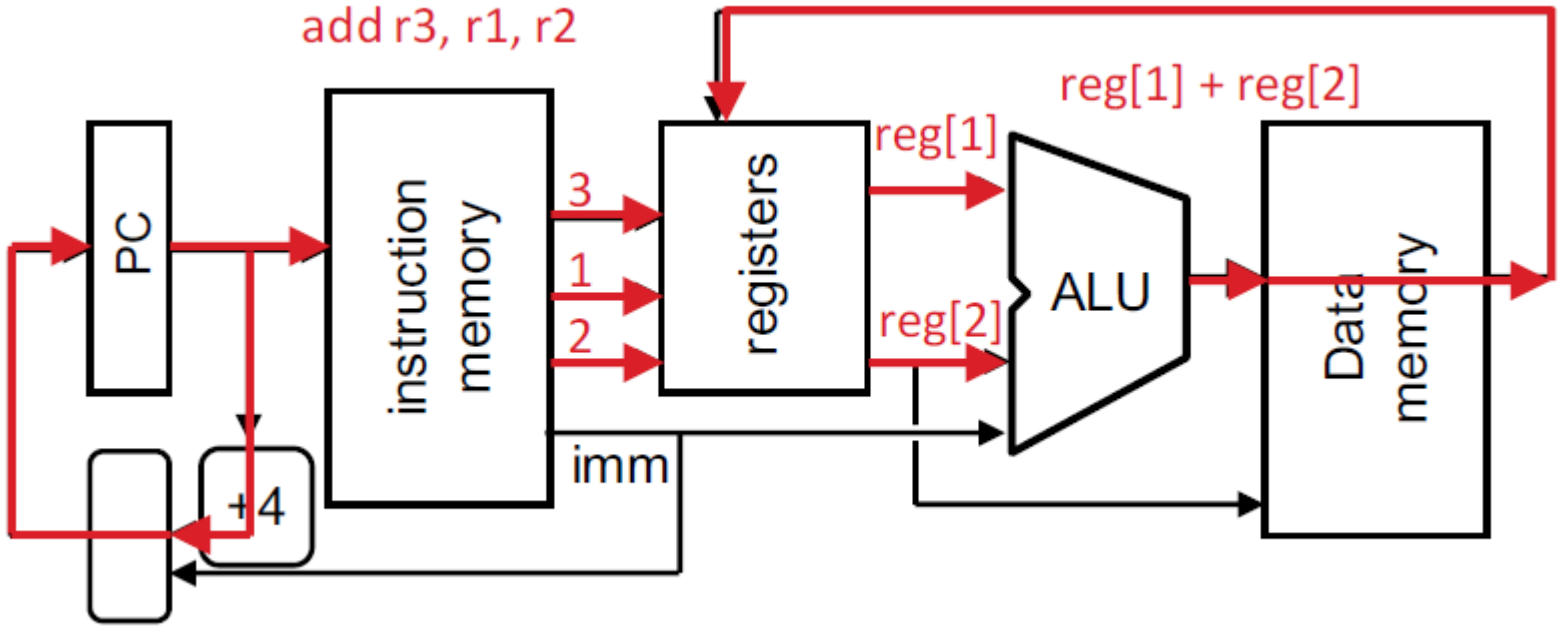


Recall five stages on datapath



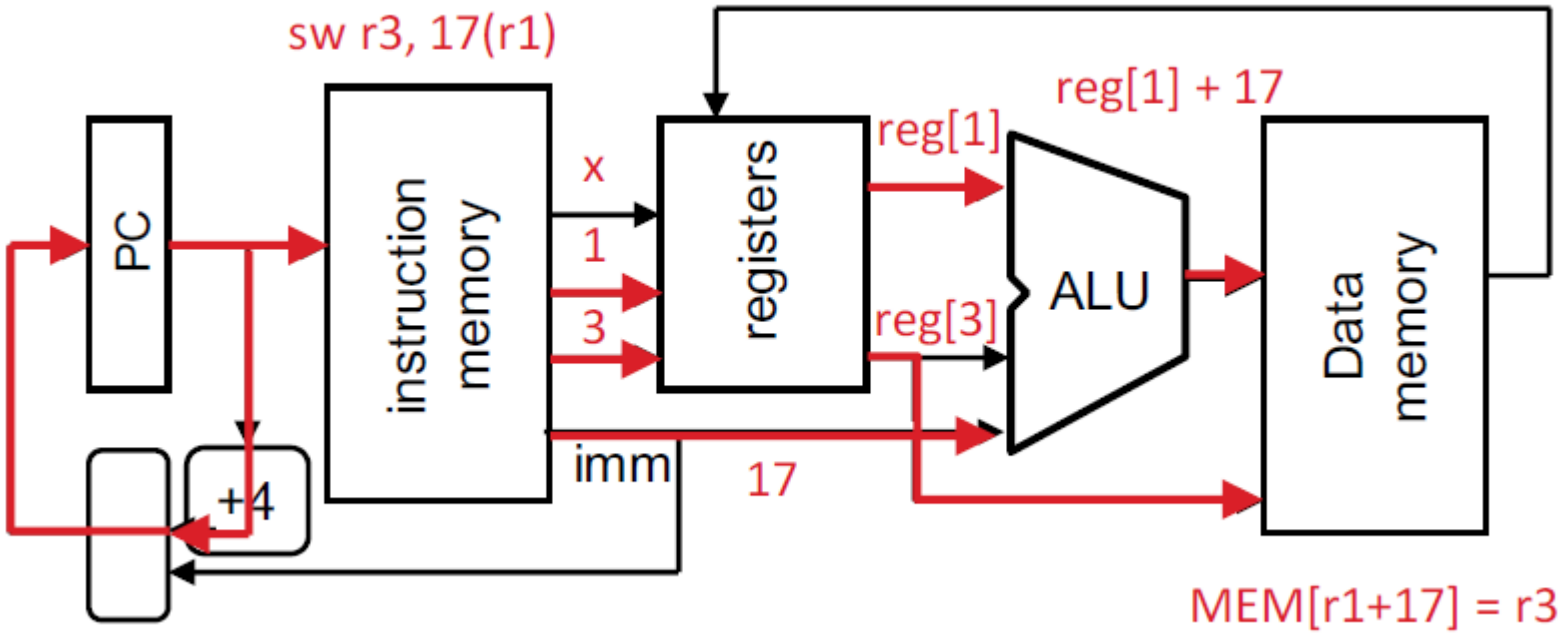
Recall Datapath Walkthroughs

- Take Add as an example



Recall Datapath Walkthroughs

- Take sw as an example



Single CPU Design

- Step1. Control signals for each operation

	Jump	Branch	RegDst	ExtOp	ALUSrc	MemWr	MemtoReg	RegWr
add								
ori								
lw								
beq								
j								

Single CPU Design

- Step1. Control signals for each operation

	Jump	Branch	RegDst	ExtOp	ALUSrc	MemWr	MemtoReg	RegWr
add	0	0	1	x	0	0	0	1
ori	0	0	0	0	1	0	0	1
lw	0	0	0	1	1	0	1	1
sw	0	0	x	1	1	1	x	0
beq	0	1	x	1	0	0	x	0
j	1	x	x	x	x	0	x	0

Single CPU to Two-Cycle CPU

How can we deal with it?

Any questions about Project 2?