Name (Pinyin):

Email:

ShanghaiTech University, Computer Architecture I 2017, HW 5

http://shtech.org/course/ca/17s/

> **Submission Information** Create a pdf (with whichever program you prefer) called ***hw5.pdf*** and commit and push it to gradebot.

Question 1 FSM and Truth Tables

You have been enlisted to design a gacha machine. The machine accepts three kinds of tokens, bronze token for 1 point, silver token for 2 points and gold token for 4 points. When 4 points have been inserted, it dispenses the gacha, and the dispenser will keepthe remaining points. Design an FSM controller for the gacha machine.

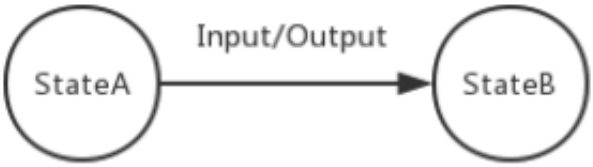
1. Implement the FSM diagram.

Requirements:

1. The FSM states and inputs are 2-bits each, while the outputs are 1-bit.
2. On each cycle, exactly one token is inserted.
3. For inputs,

   “01” -> bronze token.
   “10” -> silver token.
   “11” -> gold token.
   “00” is not existed in the input.

   Example of the FSM diagram:



ANS:

2. Represent the truth table of the FSM and use the MOST simplified SOP (Sum of Product) Expression to represent the output with state and input.

You should represent the two bit of the states individually. So as the inputs.
The result should be

Hint: Use Karnaugh map.

ANS:

1. Truth table

2. Expression

Question 2 Boolean Algebra

Simplify the following expressions.

1. $A \cdot \overline{B} + \overline{B} \cdot A + C \cdot D \cdot E + \overline{C} \cdot D \cdot E + E \cdot \overline{C} \cdot D$
2. $(A \cdot B)(L \cdot N \cdot M)(C \cdot D \cdot E)(M \cdot N \cdot L)$
3. $A \cdot (B + C) + D \cdot E + W \cdot \overline{X} + E \cdot D + \overline{X} \cdot W + (C + B) \cdot A$
4. $T \cdot (P \cdot Q + R + S \cdot T) \cdot S$
5. $\overline{\overline{DD}E}$

ANS:

1.

2.

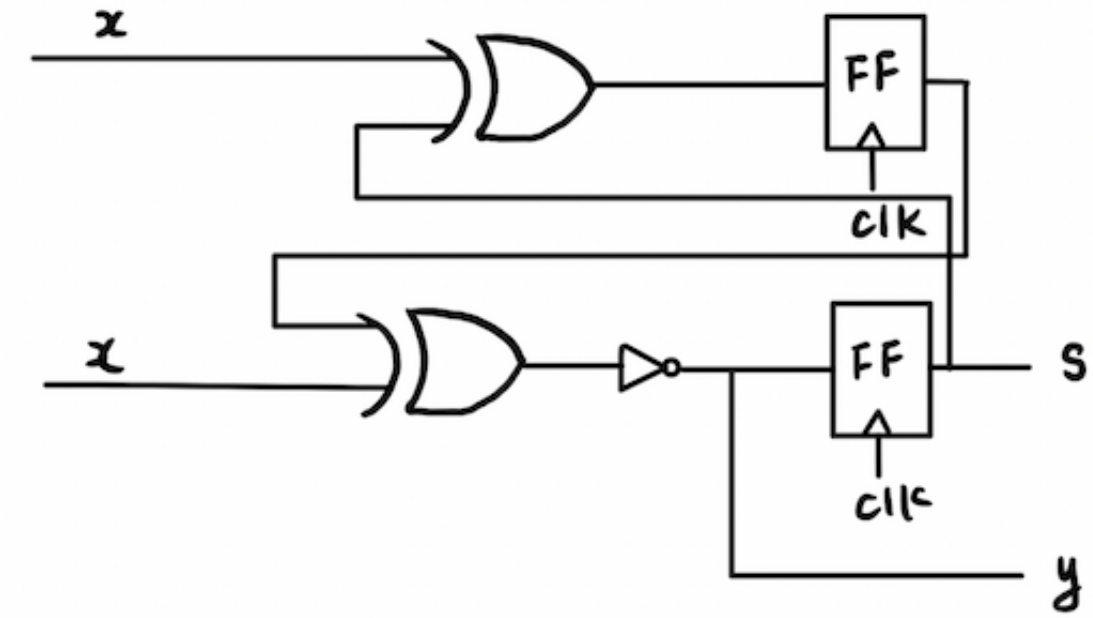
3.

4.

5.

Question 3 Timing Diagram

Consider the circuit shown below. The input is x and output is y. A clock signal is connected to each flip-flop and has a period of 6 ns. The xor gate and the inverter each have a propagation delay of 1ns. Flip-flops are positive edge-triggered and have a set-up time and clock-to-q delay of 1ns each.



Assume the flip-flips both start out storing a 0 logic value. Draw the waveforms for the output signal, y, and the signal at the node labeled s.

ANS: