Name(Pinyin): Email(Prefix):

Computer Architecture I Homework 6 2018 Spring May 15

Instructions:

Homework 6 covers the content of caches and float-points, please refer to the lecture slides. You can print it out, write on it and <u>scan</u> it into a pdf, or you can edit the PDF directly, just remember: you must create a <u>PDF</u> and upload to the <u>Gradescope</u>. Please assign the questions properly on Gradescope, otherwise you will lose 25% of points.

Tell us your feeling after finish it. Thank you!





Note: all the Miss rate & Hit rate fraction should be in the form YYY.XXXX (4 decimal)

Question Set 1. Direct Mapped Cache

[40 points] In a 16-bit machine (word size is 16 bit), the clock frequency is 2GHz. We have a cache with properties as follows:

- 1. Cache size is 4 KiB;
- 2. Block size is 1 word;
- 3. Cache hit time is 2 cycles;
- 4. Cache miss penalty is 100 cycles;

1-A. What is the width (in bits) of each field of following address bit assignment?

TAG:	Set index:	Block offset:
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Please provide info about how you came to this result. Answer 6pt + Analysis 4pt 1-B. We will access the data of addresses as follows. Fill in the blanks. It is about whether there is a hit, if miss what is the type of miss. If no miss, you need put a "/" (Hit) into the blanks "Types of miss" or just fill in it with "Compulsory", "Capacity", "Conflict". (each blank worth 1 pt.)

Addresses (serially access)	Miss or Hit {"Miss", "Hit"}	Type of Miss
0x0000		
0x0004		
0x0008		
0x000c		
0x1000		
0x1004		
0x1008		
0x100c		
0x0000		
0x0004		

1-C. Calculations. (Show progress, worth 50% pts) 1-C-i: miss rate: (4 pt.)

1-C-ii: AMAT (ns): (3 pt.)

1-C-iii: AMAT if we don't have this cache (ns): (3 pt.)

Question Set 2. Two-Way Set Associative Cache

From QS 1. We change the block size to 2 words. And implemented two-way set associative cache. The parameters are shown as follows:

- 1. Cache size is 4 KiB;
- 2. 16-bit byte-addresses machine;
- 3. Block size is 2 words;

2-A. What the width of each field of following address bit assignment:

TAG: Set index:	Block offset:
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Give me the progress how you think about it. Answer 6pt + Analysis 4pt

2-B. We will access the data of addresses as follows. Fill in the blanks. It is about whether there is a hit, if miss what is the type of miss. If no miss, you need put an "None of above" (Hit) into the blanks "Types of miss" or just fill in it with "Compulsory", "Capacity", "Conflict". (each blank worth 1 pt.)

Addresses (serially access)	Miss or Hit {"Miss", "Hit"}	Type of Miss
0x0000		
0x0004		
0x0008		
0x000c		
0x1000		
0x1004		
0x1008		
0x100c		
0x0000		
0x0004		

1-C. Calculations.

1-C-i. Miss rate: (5 pt.)

1-C-ii. Assume the new cache miss time is 110 cycles. Calculate the AMAT in ns. Round to the nearest tenth. (5 pt.)

Question Set 3. Cache Friendly Programming

This C program is run on a processor with a direct-mapped data cache with a size of 1KiB and a block size of 16 bytes.

Assume no optimization and sizeof(int) == 4 and A = 0x4000. 3-A. Calculate the miss rate. Show progress (5 pt.)

3-B-i. Rewrite the program to improve the performance. Do not use cache blocking. (4 pt.) int k, j, A[256*256];

3-B-ii. Calculate the miss rate. Show progress (5 pt.)

3-C. T/F: A write-back cache is helpful for our rewritten code from 3-B-i. (1 pt.)

Question Set 4. Floating Point Numbers

We consider the IEEE 32-bit floating point representation with a 6 bit exponent (bias of 31) and a denorm implicit exponent of -30. The significant now has 25 bits.

4-A. Convert – 38.125 to that form. In hexadecimal. (3 pt.)

4-B. Convert 0x53510000 into floating point. (3 pt.)

4-C. What is the smallest non-infinite positive integer it CANNOT represent? Explain the result. (3 pt.)

4-D. What's the smallest positive value it can represent that is not a denorm? Leave your answer as a power of 2. Explain the result. (3 pt.)

4-E. What's the smallest positive value it can represent? Leave your answer as a power of 2. Explain the result. (3 pt.)