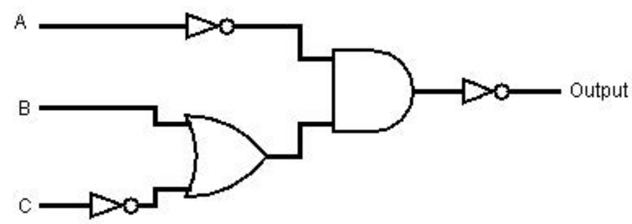
Computer Architecture Homework 4

Spring 2019, March

1 Synchronous Finite State Digital Machine Systems

a. The circuit shown below can be simplified. Write a Boolean expression that represents the function of the simplified circuit using the minimum number of AND, OR, and NOT gate.

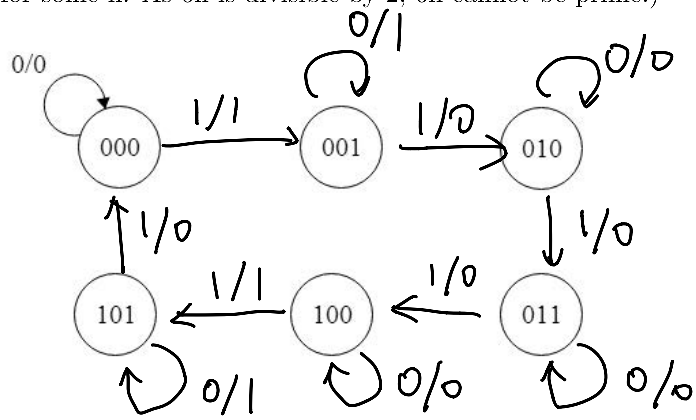


Sol: $\overline{\overline{A}\cdot(B+\overline{C})}$

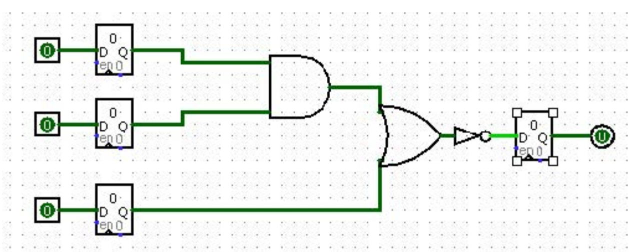
$= A + \overline{B+\overline{C}}$

$= A + \overline{B}\cdot C$

b. Consider the finite state machine below which has 6 states and a single input that can take on the value of 0 and 1. The finite state machine should output 1 IF AND ONLY IF 6 + sum of all the input values is not divisible by 2 or 3. One transition has been provided; complete the remainder of the diagram. (Hint: If the sum of the inputs is a multiple of 6, then we have 6 + sum of the inputs = 6n for some n. As 6n is divisible by 2, 6n cannot be prime.)



c. Consider the following circuit. Assume registers have a CLK to Q time of 60ps, a setup time of 40ps, and a hold time of 30ps. Assuming that all gates have the same propagation delay, what is the maximum propagation delay each individual gate could have to achieve a clock rate of 1 GHz.



Sol: 300 ps.

clock rate = 1 GHz ⇒ maximum clock period = 1000 ps.

The critical path includes: 3 combinational logic, 1 CLK-to-Q, 1 setup time.

$\Rightarrow 3 * CL + 60ps + 40ps = 1000ps.$

$\Rightarrow CL = 300ps.$

2 Boolean Logic

1. Simplify each Boolean expression to one of the following ten expressions:
$0, 1, A, B, AB, A+B, \overline{A}\,\overline{B}, \overline{A}+\overline{B}, A\overline{B}, \overline{A}B$
Each answer may be used as many times as necessary.

a. $A(A+\overline{A})+B$

$= A+B$

b. $(A+B)(\overline{A}+B)\overline{B}$

$= (AB + B\overline{A} + B)\,\overline{B}$

$= B\cdot\overline{B} = 0$

c. $\overline{\overline{A}+\overline{B}}$

$= \overline{\overline{A}}\;\overline{\overline{B}} = AB$

2. Simplify the following expression step by step (as simple as possible):

a. Standard: $(A+B)(A+\overline{B})C$

$= (A + B\overline{B})C$

$= AC$

b. Grouping & Extra Terms: $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}\,\overline{C} + ABC + A\overline{B}C$

$= \overline{A}\overline{C}(\overline{B}+B) + A\overline{C}(B+\overline{B}) + AC(B+\overline{B})$

$= \overline{A}\overline{C} + A\overline{C} + AC$

$= \overline{A}\overline{C} + A\overline{C} + A\overline{C} + AC$

$= (\overline{A}+A)\overline{C} + A(\overline{C}+C)$

$= \overline{C} + A$

c. DeMorgan's: $\overline{A(\overline{B}\,\overline{C}+BC)}$

$= \overline{A} + \overline{\overline{B}\cdot\overline{C} + BC}$

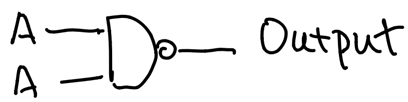
$= \overline{A} + \overline{\overline{B}\cdot\overline{C}}\;\overline{BC}$

$= \overline{A} + (B+C)(\overline{B}+\overline{C})$

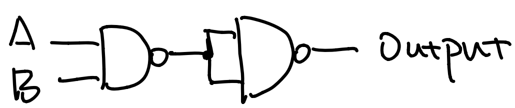
$= \overline{A} + B\overline{C} + \overline{B}C$

3 Logic Gates

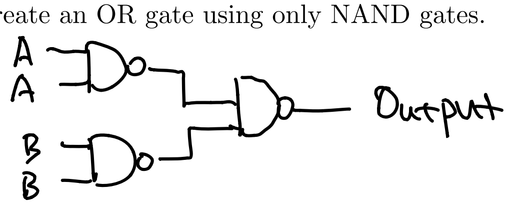
a. Create a NOT gate using only NAND gates.



b. Create an AND gate using only NAND gates. (Hint: use a)



c. Create an OR gate using only NAND gates.



d. Create a NOR gate using only NAND gates. (Hint: use a & c)