Name(Pinyin):
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# Computer Architecture Homework 6

2019 Spring Apr. 22

## Instructions:

Homework 6 is due in May. 6, covers the content of caches and float-points, please refer to the lecture slides. You can print it out and write on it, and scan it into a pdf, or you can take photos or write Latex if you want, just remember: you must create a **PDF** and upload to the **Gradescope**, please assign the questions properly on Gradescope, otherwise you will lose 25% of points.

Tell us your feeling after finish it. Thank you!

## Question Set 1. Direct Mapped Cache

[30 points] In a 16-bit byte-addresses machine, the clock frequency is 3GHz. We have a cache with properties as follows:

1. Cache size is 64 Bytes;
2. Block size is 4 Bytes;
3. Cache hit time is 2 cycles;
4. Cache miss penalty is 100 cycles;

1-A. What the width of each field of following address bit assignment:

| TAG: | Set index: | Block offset: |
|---|---|---|

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

1-B. We will access the data of addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.)

| Addresses (serially access) | Tag/Index | Hit, Compulsory or Replace |
|---|---|---|
| 0x0000 | | |
| 0x0004 | | |
| 0x0008 | | |
| 0x000c | | |
| 0x1000 | | |
| 0x1004 | | |
| 0x1008 | | |
| 0x100c | | |
| 0x0000 | | |
| 0x0004 | | |

1-C. Calculations. (Step-by-step, worth 50% pts)
1-C-i: Miss rate: (4 pt.)

1-C-ii: AMAT (ns): (3 pt.)

1-C-iii: AMAT if we don't have this cache (ns): (3 pt.)

## Question Set 2. Two-Way Set Associative Cache

From QS 1. We change the block size to 8 Bytes and implemented a two-way set associative cache. The parameters are shown as follows:

1. Cache size is 64 Bytes;
2. 16-bit byte-addresses machine;
3. Block size is 2 words;

2-A. What is the width of each field of following address bit assignment? :

| TAG: | Set index: | Block offset: |
|---|---|---|

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

2-B. We will access the data of the addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.)

| Addresses (serially access) | Tag/Index | Hit, Compulsory or Replace |
|---|---|---|
| 0x0000 | | |
| 0x0004 | | |
| 0x0008 | | |
| 0x000c | | |
| 0x1000 | | |
| 0x1004 | | |
| 0x0000 | | |
| 0x0100 | | |
| 0x0000 | | |
| 0x1004 | | |

2-C. Calculations.
2-C-i. Miss rate: (5 pt.)

2-C-ii. Assume the new cache miss time is 200 cycles and hit time is 3 cycles. Calculate the AMAT in ns. Round to the nearest tenth. (5 pt.)

## Question Set 3. Floating Point Numbers

We consider the IEEE 32-bit floating point representation except with a 7-bit exponent (bias of 63) and a denorm implicit exponent of -62.
3-A. Convert `-95.2` to that form. In hexadecimal.

3-B. Convert `0x4a23a000` into a floating point number, specify infinities as `+inf` and `-inf`, and not a number as `NaN`.

3-C. What is the smallest non-infinite positive integer it CANNOT represent? (an integer is `XX.0000`). Please explain why.

3-D. What's the smallest positive value it can represent that is not a denorm? Leave your answer as a power of 2. Please explain why.

3-E. What's the smallest positive value it can represent? Leave your answer as a power of 2. Please explain why.