CS 110 Computer Architecture

Summary

Instructors: Sören Schwertfeger & Chundong Wang

https://robotics.shanghaitech.edu.cn/courses/ca/21s/

School of Information Science and Technology SIST

ShanghaiTech University

Slides based on UC Berkley's CS61C

Final Exam

- Date: Thursday, June 17th, 2021
- Time: 10:30am 12:30pm
 - Be there latest 10:15 we start at 10:30 sharp!
- Venue: <u>check on egate which room you will be in</u>!
 - 教学中心101 教学中心201
- Closed book:
 - You can bring <u>three</u> A4 pages with notes (both sides; in <u>English</u>): Write your Chinese and Pinyin name on the top! <u>Handwritten</u> by you!
 - <u>"Written on iPAD/Surface/..., printed out" NOT allowed!!!</u>
 - You will be provided with the RISC-V "green sheet"
 - No other material allowed!

Final Exam

- Switch cell phones off! (not silent mode – off!)
 - Put them in your bags.
- Bags away from you. Nothing except paper, pen, 1 drink, 1 snack, your student ID card on the table!
- No other electronic devices are allowed!
 - No ear plugs, music, smartwatch...
- Anybody touching any electronic device will FAIL the course!
- Anybody found cheating (copy your neighbors answers, additional material, ...) will **FAIL** the course!
- Content: Everything!









COMPUTER RGANIZATION THE HALLWARE/SOFTWATCH INTERFACE



DAVID A. PATTERSON JOHN L. HENNESSY

Admin

FUNCTIONS OF SEVERAL VARIARIES Z= f(x,u) w= f(x,u,z)	DOMANNE: Allowed (Scu), (N.V. 2) PANGES: 2544
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39 by by by2 by2 by2 by by be = a2 by Equation	INCREMENTS bx, by, bz DIFFERENTIAUS, dx, dy, da
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I. Find values of f at the critical points of f in D	HIGHER D FUNCTION IS 1 TO YOUR SUPPORT
. Find the extreme values of f on the Boundary of D	2 7 to x2+42+2=1 Lot W= x2+42+22-1
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Admin

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Let us review CA now.

New School Computer Architecture (1/3)

Personal Mobile Devices

New School Computer Architecture (2/3)

warehouse-scale computer

power substation

14

cooling

towers



Old Machine Structures



New-School Machine Structures (It's a bit more complicated!)

- Software Parallel Requests Assigned to computer e.g., Search "Katz"
- Parallel Threads
 Assigned to core
 e.g., Lookup, Ads
- Parallel Instructions

 >1 instruction @ one time
 e.g., 5 pipelined instructions
- Parallel Data

>1 data item @ one time e.g., Add of 4 pairs of words

- Hardware descriptions
 All gates functioning in parallel at same time
- Programming Languages



Great Ideas in Computer Architecture

- 1. Design for Moore's Law
- 2. Abstraction to Simplify Design
- 3. Make the Common Case Fast
- 4. Dependability via Redundancy
- 5. Memory Hierarchy
- 6. Performance via Parallelism/Pipelining/Prediction

Powers of Ten inspired CA Overview

Going Top-Down cover 3 Views

- 1. Architecture (when possible)
- 2. Physical Implementation of that architecture
- 3. Programming system for that architecture and implementation (when possible)

• See <u>http://www.powersof10.com/film</u>

Earth

10⁷ meters





10⁷ meters



10⁶ meters



The Dalles, Oregon ¹⁰⁴ meters



The Dalles, Oregon ^{10⁴} meters



Google's Oregon WSC 10³ meters



Google's Oregon WSC 10⁴ meters



Google Warehouse

- 90 meters by 75 meters, 10 Megawatts
- Contains 40,000 servers, 190,000 disks
- Power Utilization Effectiveness: 1.23
 - 85% of 0.23 overhead goes to cooling losses
 - 15% of 0.23 overhead goes to power losses
- Contains 45, 40-foot long containers

-8 feet \times 9.5 feet \times 40 feet

• 30 stacked as double layer, 15 as single layer

Containers in WSCs ^{10²} meters



Google Container



10¹ meters

Google Container





- 2 long rows, each with 29 racks
- Cooling below raised floor
- Hot air returned behind racks

10⁰ meters

Equipment Inside a Container

Server (in rack format):





Array (aka cluster): server racks + larger local area network switch ("array switch") 10X faster => cost 100X: cost f(N²) 32

Great Ideas in Computer Architecture

- 1. Design for Moore's Law
 - -- WSC, Container, Rack
- 2. Abstraction to Simplify Design
- 3. Make the Common Case Fast
- 4. Dependability via Redundancy -- Multiple WSCs, Multiple Racks, Multiple Switches
- 5. Memory Hierarchy
- 6. Performance via Parallelism/Pipelining/Prediction
 - -- Task level Parallelism, Data Level Parallelism

Google Server Internals¹⁰⁻¹ meters



Software: Often uses MapReduce

- Simple data-parallel *programming model* and *implementation* for processing large datasets
- Users specify the computation in terms of
 - a *map* function, and
 - a *reduce* function
- Underlying runtime system
 - Automatically *parallelize* the computation across large scale clusters of machines
 - Handles machine failure
 - Schedule inter-machine communication to make efficient use of the networks

Programming Multicore Microprocessor: OpenMP

```
#include <omp.h>
#include <stdio.h>
static long num steps = 100000;
int value[num steps];
int reduce()
ł
  int i;
  int sum = 0;
#pragma omp parallel for private(x) reduction(+:sum)
  for (i=1; i<= num steps; i++) {</pre>
       sum = sum + value[i];
```

Great Ideas in Computer Architecture

- 1. Design for Moore's Law
 - -- More transistors = Multicore + SIMD
- 2. Abstraction to Simplify Design
- 3. Make the Common Case Fast
- 4. Dependability via Redundancy
- 5. *Memory Hierarchy*
 - -- More transistors = Cache Memories
- 6. *Performance via Parallelism/Pipelining/ Prediction*
 - -- Thread-level Parallelism

AMD Opteron Microprocessor



centimeters

10⁻² meters

AMD Opteron Microarchitecture



AMD Opteron Pipeline Flow

• For integer operations



12 stages (Floating Point is 17 stages)
Up to 106 RISC-ops in progress

AMD Opteron Block Diagram



10⁻² meters AMD Opteron Microprocessor



10⁻³ meters

AMD Opteron Core



10⁻³ meters

AMD Opteron Core



Programming One Core: C with Intrinsics

void mmult(int n, float *A, float *B, float *C)
{
 for (int i = 0; i < n; i+=4)
 for (int j = 0; j < n; j++)</pre>

Inner loop from gcc –O -S Assembly snippet from innermost loop:

movaps (%rax), %xmm9 mulps %xmm0, %xmm9 addps %xmm9, %xmm8 movaps 16(%rax), %xmm9 mulps %xmm0, %xmm9 addps %xmm9, %xmm7 movaps 32(%rax), %xmm9 mulps %xmm0, %xmm9 addps %xmm9, %xmm6 movaps 48(%rax), %xmm9 mulps %xmm0, %xmm9 addps %xmm9, %xmm5

Great Ideas in Computer Architecture

- 1. Design for Moore's Law
- 2. Abstraction to Simplify Design
 - -- Instruction Set Architecture, Micro-operations
- 3. Make the Common Case Fast
- 4. Dependability via Redundancy
- 5. Memory Hierarchy
- 6. Performance via Parallelism/Pipelining/Prediction
 - -- Instruction-level Parallelism (superscalar, pipelining)
 - -- Data-level Parallelism

SIMD Adder

- Four 32-bit adders that operate in parallel
 - Data Level Parallelism



One 32-bit Adder



1 bit of 32-bit Adder



Complementary MOS Transistors (NMOS and PMOS) of NAND Gate



×	У	Z
0 volts	0 volts	3 volts
0 volts	3 volts	3 volts
3 volts	0 volts	3 volts
3 volts	3 volts	0 volts

Physical Layout of NAND Gate 10-7 meters

100 nanometers



Scanning Electron Microscope



Top View



10⁻⁷ meters

Cross Section

10⁻⁶ meters Block Diagram of Static RAM



1 Bit SRAM in 6 Transistors



Physical Layout of SRAM Bit



10⁻⁷ meters

10⁻⁷ meters

SRAM Cross Section





DIMM Module

- DDR = Double Data Rate
 - Transfers bits on Falling AND Rising Clock Edge
- Has Single Error Correcting, Double Error Detecting Redundancy (SEC/DED)
 - 72 bits to store 64 bits of data
 - Uses "Chip kill" organization so that if single
 DRAM chip fails can still detect failure
- Average server has 22,000 correctable errors and 1 uncorrectable error per year

10⁻⁶ meters

DRAM Bits



1 micron

DRAM Cell in Transistors



Physical Layout of DRAM Bit



Cross Section of DRAM Bits



100 nanometers

10⁻⁷ meters

AMD Opteron Dependability

- L1 cache data is SEC/DED protected
- L2 cache and tags are SEC/DED protected
- DRAM is SEC/DED protected with chipkill
- On-chip and off-chip ECC protected arrays include autonomous, background hardware scrubbers
- Remaining arrays are parity protected
 - Instruction cache, tags and TLBs
 - Data tags and TLBs
 - Generally read only data that can be recovered from lower levels

Programming Memory Hierarchy: Cache Blocked Algorithm

• The blocked version of the i-j-k algorithm is written simply as (A,B,C are submatricies of a, b, c)

- r = block (sub-matrix) size (Assume r divides N)
- X[i][j] = a sub-matrix of X, defined by block row i and block column j

Great Ideas in Computer Architecture

- 1. Design for Moore's Law
 - -- Higher capacities caches and DRAM
- 2. Abstraction to Simplify Design
- 3. Make the Common Case Fast
- 4. Dependability via Redundancy -- Parity, SEC/DEC
- 5. Memory Hierarchy
 - -- Caches, TLBs
- 6. Performance via Parallelism/Pipelining/Prediction
 - -- Data-level Parallelism

Course Summary

- As the field changes, Computer Architecture courses change, too!
- It is still about the software-hardware interface
 - Programming for performance!
 - Parallelism: Task-, Thread-, Instruction-, and Data-MapReduce, OpenMP, C, SSE Intrinsics
 - Understanding the memory hierarchy and its impact on application performance