Computer Architecture Homework 4

Spring 2022, April

1 Boolean Algebra and Logic Gates

Question 1.1

For the following function:

bool fun(bool A, bool B) return (A == B) ? true : B;

a. Write the Truth Table of it.(5 pts)

b. Write the Boolean Expression of it and simplify it (as simple as possible).(10 pts)

c. Draw the gate diagram that implements the boolean expression in b.(5 pts)

Solution:

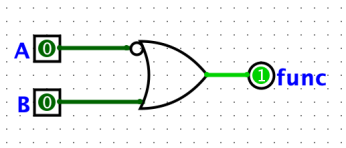
a.

A	B	fun(A,B)
FALSE	FALSE	TRUE
FALSE	TRUE	TRUE
TRUE	FALSE	FALSE
TRUE	TRUE	TRUE

b. $\overline{A}$+B

Please be familiar with Laws of Boolean Algebra

c.



Please using Gates and use the notation learned in the class

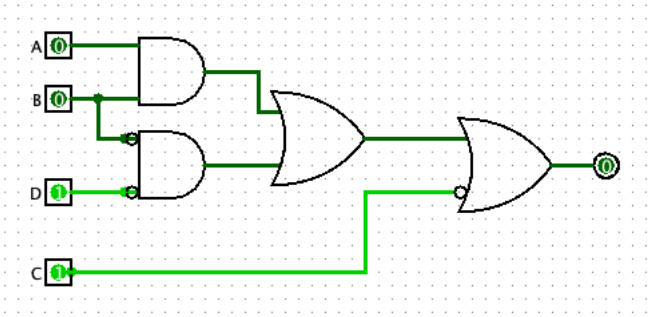
Question 1.2

a. Simplify the following Boolean Expressions (as simple as possible and show enough steps please).(15 pts)

$$
\begin{aligned}
& B(AB + A\overline{B})(\overline{AC} + C) + \overline{CC} + (A + \overline{B})(\overline{CD}) \\
=& B(AB + A\overline{B})(\overline{AC} + C) + \overline{CC} + (A + \overline{B})(\overline{C} + \overline{D}) \\
=& BA(1) + \overline{C} + A\overline{C} + A\overline{D} + \overline{B}\ \overline{C} + \overline{B}\ \overline{D} \\
=& AB + \overline{C} + A\overline{D} + \overline{B}\ \overline{D} \qquad (1) \\
=& AB + \overline{C} + A\overline{D}(B + \overline{B}) + \overline{B}\ \overline{D} \qquad \text{(introduce } B + \overline{B}\text{)} \\
=& AB + \overline{C} + A\overline{D}B + A\overline{DB} + \overline{B}\ \overline{D} \\
=& AB + \overline{C} + \overline{B}\ \overline{D}
\end{aligned}
$$

Please be familiar with Lecture_10 P30 Laws of Boolean Algebra
Be careful about $\overline{XX}$ and $\overline{X}\ \overline{X}$

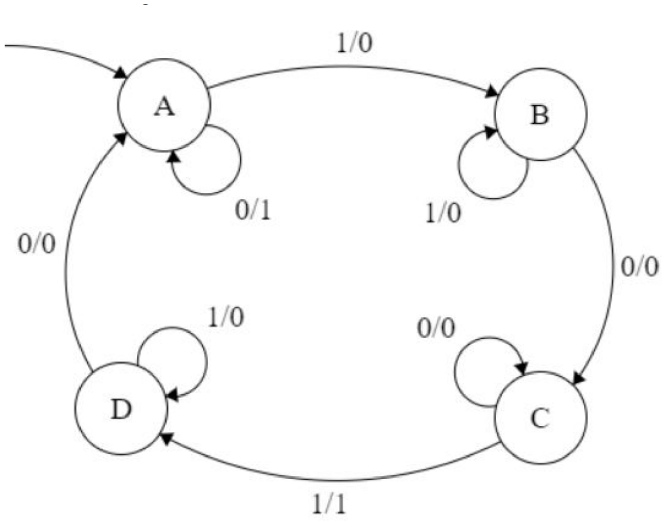
b. Draw the circuit according to the simplified boolean expression in (a) . (10 pts)



2 FSM

Question 2

For the following Finite State Machine, fill out the remainder of the table. (15 pts)



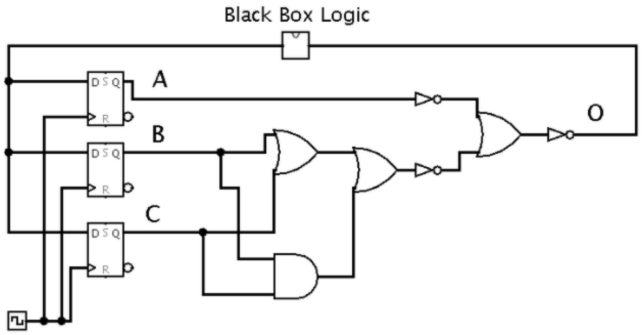
Input	-	1	0	0	1	1	0	0	0
Next State	A	B	C	C	D	D	A	A	A
Output	-	0	0	0	1	0	0	1	1

Table 1: Write Answer Here

3 SDS

Question 3

In the following circuit, NOT gates have a delay of 3ns, AND and OR gates have a delay of 7ns, and the "Black Box" logic component has a delay of 9ns. The registers have a clk-to-q delay of 6ns and setup times of 5ns.



a. What is the maximum allowable hold time of the registers? (please include enough explanation) (20 pts)

28ns:

The shortest path through the circuit to a register clearly follows the path from A to O and includes: clk-to-q delay, two NOT gates, one OR gate, and the "Black Box." Maximum hold time = 6 + 2*3 + 7 + 9 = 28ns

b. What is the minimum acceptable clock period for this circuit? (please include enough explanation) (20 pts)

47ns:

The period is determined by the longest path and includes: clk-to-q delay, two NOT gates, three OR gates (or two OR gates and one AND gate), the "Black Box", and the setup time. Minimum period = 6 + 2*3 + 3*7 + 9 + 5 = 47ns