Question 2 Boolean Algebra

Simplify the following expressions.

1. $A \cdot \overline{B} + \overline{B} \cdot A + C \cdot D \cdot E + \overline{C} \cdot D \cdot E + E \cdot \overline{C} \cdot D$
2. $(A \cdot B)(L \cdot N \cdot M)(C \cdot D \cdot E)(M \cdot N \cdot L)$
3. $A \cdot (B + C) + D \cdot E + W \cdot \overline{X} + E \cdot D + \overline{X} \cdot W + (C + B) \cdot A$
4. $T \cdot (P \cdot Q + R + S \cdot T) \cdot S$
5. $\overline{\overline{DD}E}$

Solution:

Simplify the following expressions.

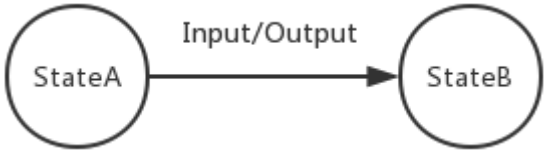
1. $A \cdot \overline{B} + C \cdot D \cdot E + \overline{C} \cdot D \cdot E$
2. $(A \cdot B)(L \cdot N \cdot M)(C \cdot D \cdot E)$
3. $A \cdot (B + C) + D \cdot E + W \cdot \overline{X}$
4. $T \cdot S$
5. $D + \overline{E}$

Question #: FSM and Truth Tables

You have been enlisted to design a gacha machine. The machine accepts three kinds of tokens, bronze token for 1 point, silver token for 2 points and gold token for 4 points. When 4 points have been inserted, it dispenses the gacha, and the dispenser will keep the remaining points. Design an FSM controller for the gacha machine.

1. **Implement the FSM diagram.**
   Requirements:
   1. The FSM states and inputs are 2-bits each, while the outputs are 1-bit.
   2. On each cycle, exactly one token is inserted.
   3. For inputs,
      "01" -> bronze token.
      "10" -> silver token.
      "11" -> gold token.
      "00" is not existed in the input.

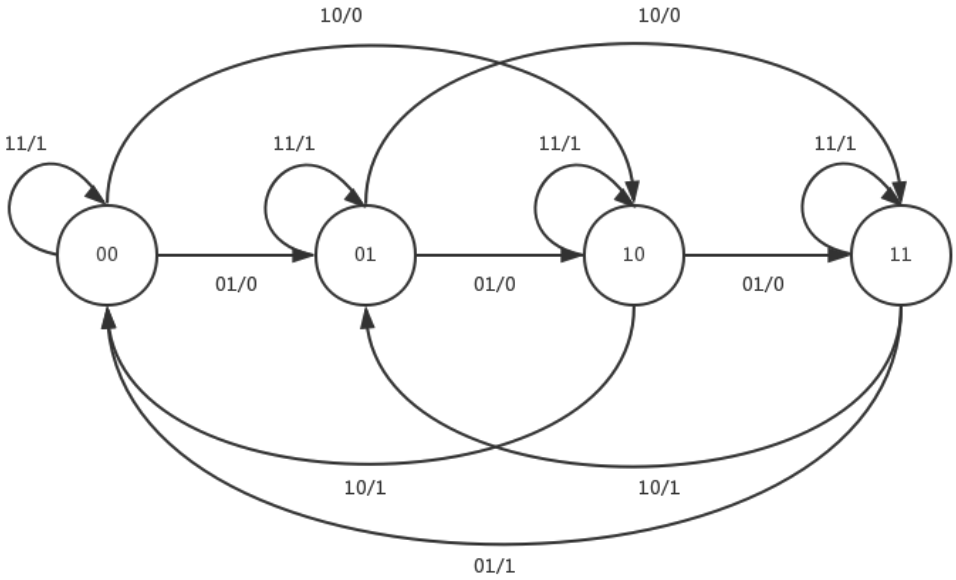
   Example of the FSM diagram:



2. **Represent the truth table of the FSM and use the MOST simplified SOP (Sum of Product) Expression to represent the output with state and input.**
   You should represent the two bit of the states individually. So as the inputs.
   The result should be
   Hint: Use Karnaugh map.

Solution

1.



2. Truth Table

StateA		Input		StateB		Output
st1	st0	in1	in0	st1	st0	
0	0	0	1	0	1	0
		1	0	1	0	0
		1	1	0	0	1
0	1	0	1	1	0	0
		1	0	1	1	0
		1	1	0	1	1
1	0	0	1	1	1	0
		1	0	0	0	1
		1	1	1	0	1
1	1	0	1	0	0	1
		1	0	0	1	1
		1	1	1	1	1

Karnaugh Map (Not Necessary)

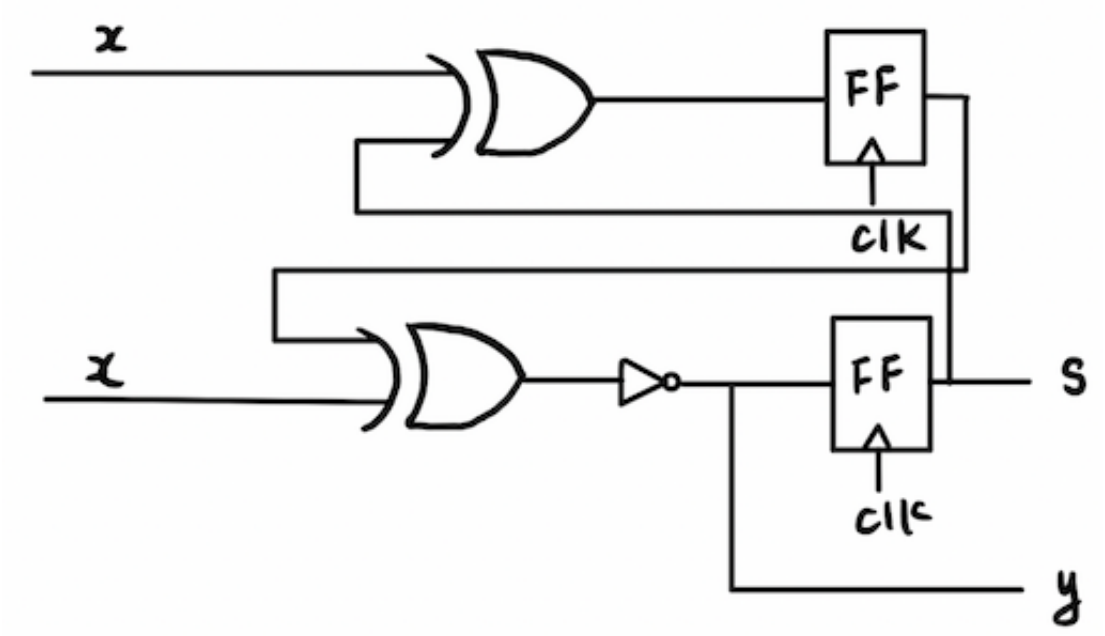
st/in	00	01	11	10
00	X	0	1	0
01	X	0	1	0
11	X	1	1	1
10	X	0	1	1

Boolean Expression:

$$(\mathrm{st0} * \mathrm{st1}) + (\mathrm{in0} * \mathrm{in1}) + (\mathrm{st1} * \mathrm{in1})$$

Question 3 Timing Diagram

Consider the circuit shown below. The input is x and output is y. A clock signal is connected to each flip-flop and has a period of 6 ns. The xor gate and the inverter each have a propagation delay of 1ns. Flip-flops are positive edge-triggered and have a set-up time and clock-to-q delay of 1ns each.



Assume the flip-flips both start out storing a 0 logic value. Draw the waveforms for the output signal, y, and the signal at the node labeled s.

ANS: