Discussion 6: SDS

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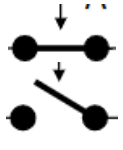
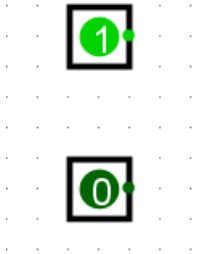
Synchronous Digital Systems

- Synchronous:
  - All operations coordinated by a central clock

- Digital:
  - Represent all values by 1 and 0
  - High voltage(V_{dd}) = True = On switch = 1
  - Low voltage (0V) = False = Off switch = 0

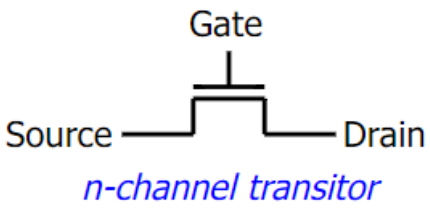




- Synchronous Digital Systems consist of two basic types of circuits:
  - Combinational Logic (CL) circuits
  - Sequential Logic (SL)

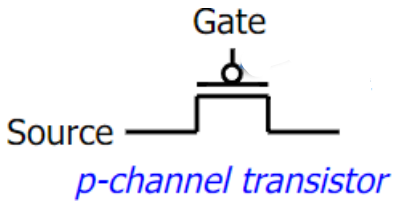
CMOS Transistor Networks

Negative



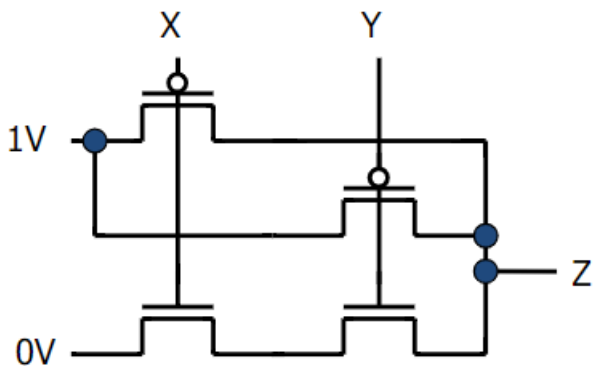
Off when voltage at Gate is low
On when voltage(Gate) > voltage (Threshold)
Can pass 0V when Gate is 1V

Positive



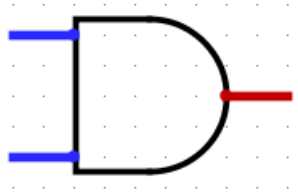
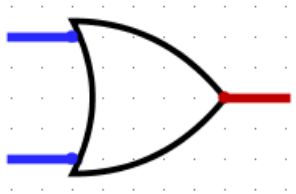
On when voltage at Gate is low
Off when voltage(Gate) > voltage (Threshold)
Can pass 1V when Gate is 0V

CMOS Networks



X	Y	Z
1	1	0
1	0	1
0	1	1
0	0	1

Combinational Logic

AND	$A \cdot B$	
OR	$A + B$	
NOT	$\overline{A}$	

Truth Table

- Same as Discrete Mathematics
- Single bit input

A	B	C
1	1	0
1	0	1
0	1	1
0	0	0

- Multiple bit input

A	B	C
a_1a_0	b_1b_0	$c_2c_1c_0$

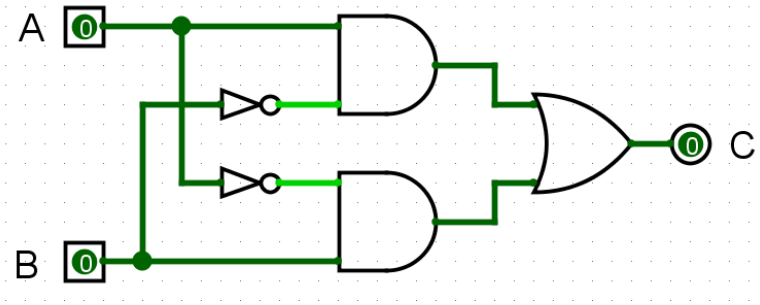
From Truth Table to logical expression

- Sum of Products form (AKA Principal Disjunctive Normal Form in Discrete Mathematics)
  - $C = A \cdot \bar{B} + \bar{A} \cdot B$
- This will help you simplify an unknown logic.
- Also you can use Product of Sums(AKA PCNF)
  - $C = (A + B) \cdot (\bar{A} + \bar{B})$
- Do not forget to use Laws of Boolean Algebra.

$X\overline{X} = 0$	$X + \overline{X} = 1$	Complementarity
$X\ 0 = 0$	$X + 1 = 1$	Laws of 0's and 1's
$X\ 1 = X$	$X + 0 = X$	Identities
$X\ X = X$	$X + X = X$	Idempotent Laws
$X\ Y = Y\ X$	$X + Y = Y + X$	Commutativity
$(X\ Y)\ Z = X\ (Y\ Z)$	$(X + Y) + Z = X + (Y + Z)$	Associativity
$X\ (Y + Z) = X\ Y + X\ Z$	$X + Y\ Z = (X + Y)\ (X + Z)$	Distribution
$X\ Y + X = X$	$(X + Y)\ X = X$	Uniting Theorem
$\overline{X}\ Y + X = X + Y$	$(\overline{X} + Y)\ X = X\ Y$	Uniting Theorem v. 2
$\overline{X\ Y} = \overline{X} + \overline{Y}$	$\overline{X + Y} = \overline{X}\ \overline{Y}$	DeMorgan's Law

Representations of Combinational Logic

Gate Diagram



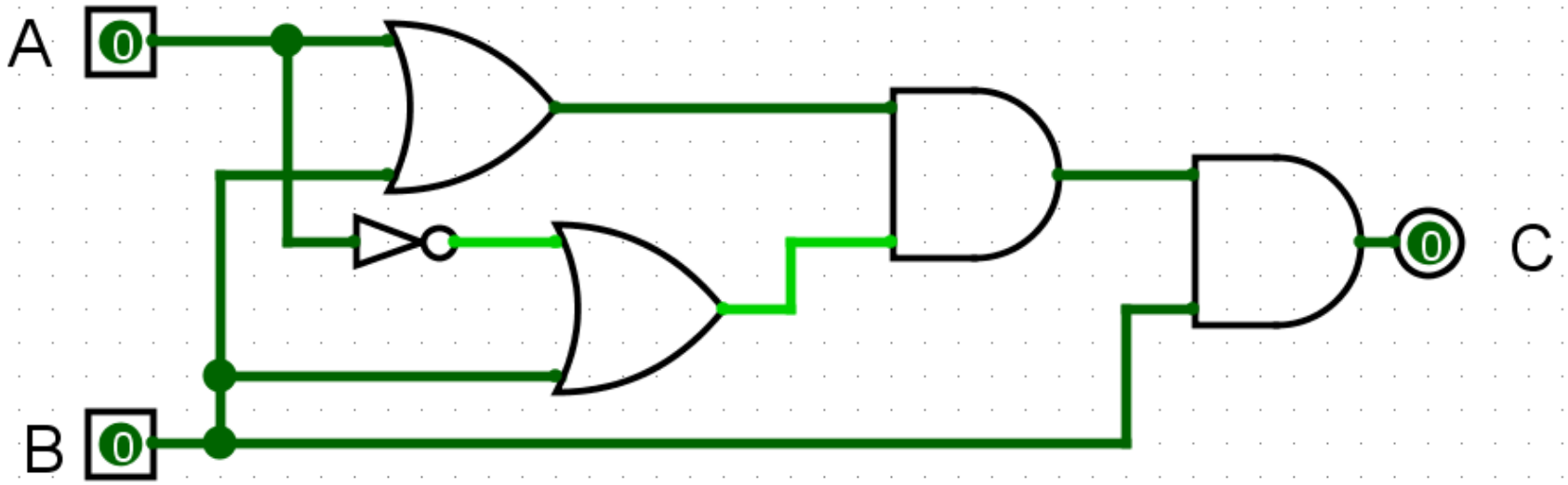
Boolean Expression

$$C = A \cdot \bar{B} + \bar{A} \cdot B$$

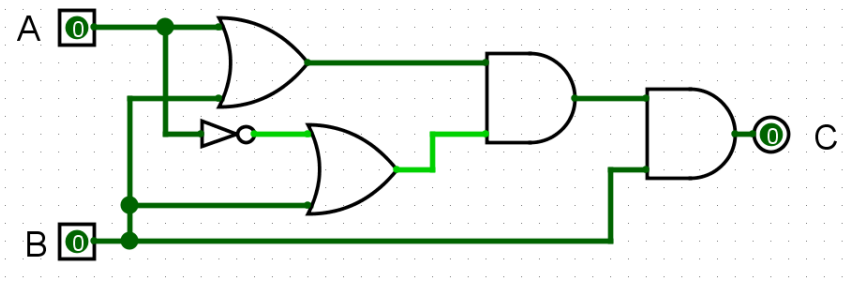
Truth Table

A	B	C
1	1	0
1	0	1
0	1	1
0	0	0

Example



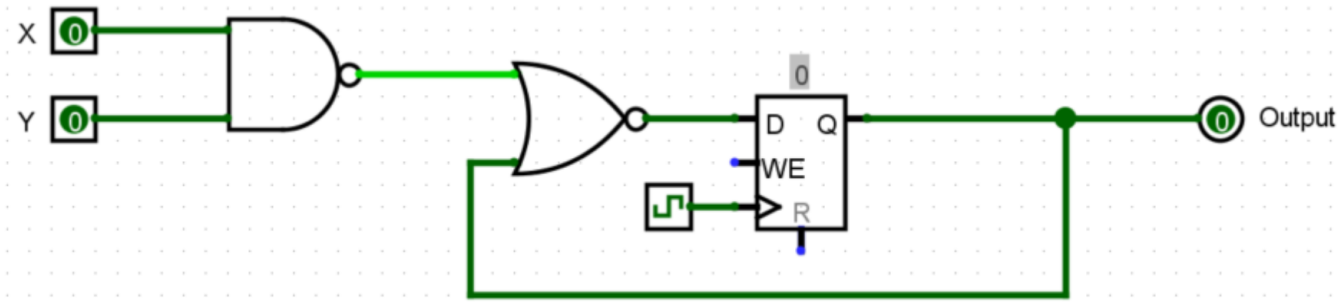
Example



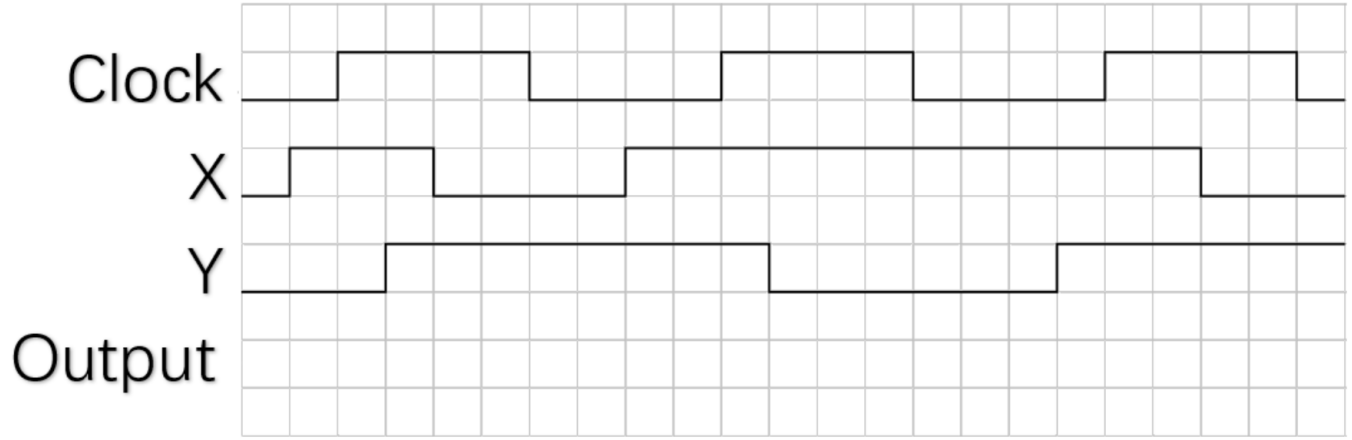
$$
\begin{aligned}
C &= (A + B) \cdot (\bar{A} + B) \cdot B \\
&= (A \cdot \bar{A} + B \cdot \bar{A} + A \cdot B + B \cdot B) \cdot B \\
&= (B \cdot (\bar{A} + A) + B) \cdot B \\
&= (B + B) \cdot B \\
&= B \cdot B \\
&= B
\end{aligned}
$$

7. **SDS**

(a) Draw the Timing Diagram for the circuit below. The delay for the gates are 10 ns, the clock-to-q delay for a register is 20 ns, each clock cycle is 80 ns, each grid in the following diagram is a unit of 10 ns. The output is initially given in the graph.



Use any of those graphs to put in your answer (so you can re-do it). Clearly mark your final answer if you use more than one graph!



8. **Circuit time calculation**

In this circuit below, RegA and RegB have setup, hold and clk-to-q times of 8ns, NOT logic gate has a delay of 1ns, AND logic gate has a delay of 3ns, XNOR logic gate has a delay of 5ns, and RegC has a setup time of 9ns.